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MANUFACTURING METHOD FOR A SEMICONDUCTOR DEVICE
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Specifications /125*

1. Title of the Invention

Manufacturing method for a semiconductor device

2. Claims

(1) A manufacturing method for a semiconductor device comprised of a silicide gas such as silane or dichlorosilane as the primary reactive gas; a carbide, nitride or oxide gas such as methane, ammonium or oxygen as the secondary reactive gas additive; and a phosphine, arsine or diborane as the tertiary reactive gas that functions as the impurities for the electrically conductive semiconductor
that involves a process to form a primary amorphous semiconductor containing hydrogen or halogen elements due to high frequency heating at 1-50MHz using a substrate temperature from room temperature to 500°C, and
that has a secondary amorphous semiconductor with a PN, PI or NI junction that is layered on top of the aforementioned amorphous semiconductor, and
where either the primary or secondary amorphous semiconductor has varying weights or types when compared to the secondary reactive gas additive used in forming the secondary or the primary amorphous semiconductor.

3. Detailed Explanation of the Invention

[Industrial Field of the Invention]

This invention relates to a manufacturing method for a semiconductor device formed of an amorphous or polycrystalline

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semiconductor with an additive of hydrogen or halogen elements that are electrically conductive, followed by an amorphous semiconductor layered on top that is comprised of an amorphous or polycrystalline hydrogen or halogen additive that has varying types of electrical conductivity to alter the energy bands.

The substrate for this invention involves a semiconductor that has either an amorphous (pure amorphous or 5-100A short range order polycrystalline) such as silicon, germanium or silicon carbide that is electrically conductive, or a polycrystalline structure, and that has uniform dispersion of carbon, oxygen or nitrogen (hereafter abbreviated as amorphous semiconductor).

The uniform dispersion in this invention refers to a localized reciprocal action created via quantum theorized wave movement of additives. /126

This silicon, germanium or silicon carbide amorphous or polycrystalline semiconductor and carbon, oxygen or nitrogen additive creates a semiconductor with a uniform crystalline structure that has uniform additive dispersion. This relates to the semiconductor with varying energy gaps where there is continuous change in the energy bands in the boundary or surrounding areas. There is a PN or PIN junction in the boundary or surrounding areas that is subject to exposure that generates photovoltaic force.

Currently, if there is a boundary around the semiconductor with varying energy bands, this boundary has a configuration called a heterojunction. For example, with a junction of Gal and GaAs that is a single crystal, the boundary of these two energy gaps (hereafter, Eg) is as shown in Fig. 1, where there is an incommensurate abrupt

heterojunction. Because it is incommensurate, intervalence states are generated at other junctions such as $Ca_{0.3}AlAs$ (1) and GaAs (2), conduction bands (9), notches (3), valence bands (10) or lifts (4). Due to these interface states (hereafter Ns), electrons or hole carriers fluctuate at both junctions as a result.

As a result, the life of the carrier is reduced and particular operations using this junction, such as a decrease in the photovoltaic load when generating photovoltaic force, cause tremendous problems. Also, if there are semiconductor PN junction diode properties, the reverse pressure weakens and it becomes a soft diode. Figure 1 (A) shows the common Fermi level (10) of the N-type semiconductor and P-type semiconductor (2), with the disconnected N-P junction at the conduction band (8) and valence band (9). On the other hand, with an N-N junction configuration of an N-type semiconductor (1) and another N-type semiconductor (7), the spike (6) generated is greater than the Ns (5), as illustrated in Fig. 1 (B). Thus, there is a huge problem with electron migration. This invention prevents the generation of notches, lift and spikes. A primary objective is to continuously vary the energy bands in this junction. This invention is capable of eliminating or drastically reducing the generation of Ns that are the cause of bond failure and crystalline defects existing due to the lack of a crystal lattice at the interface with the heterojunction. With energy bands at a continuous junction, the variance in energy bands had made development of a new semiconductor device proceed rapidly.

The following is a description of this invention, based on the embodiment examples.

When the semiconductor is formed using a coating on a composite substrate applied to all or part of a metallic film on an insulator such as glass or ceramic, the semiconductor materials can include a coating such as silane, dichlorosilane or other silicide gases. Silane, dichlorosilane or other silicide gases, carrier gases such as hydrogen or hydrogen chloride and conductive impurities such as phosphorus, arsenic or boron were added to the phosphine, arsine or diborane at the opening of the quartz heat-resistant glass or stainless steel reactor. Next, carbide, nitride and oxide gases such as methane, ammonia and oxygen were added. Discharge was conducted using a vacuum pump until the pressure inside the reactor was 0.001torr. The substrate was held in a susceptor inside the reactor until the reactor was at 0.1-10torr. 1-50MHz of high-frequency heating, or that combined with wide range heating was conducted and the reactive gases were subject to excitation or dispersion. These reactive gases formed a coating on the substrate. At this point, the coating was amorphous when the temperature of the coating was between room temperature and 500°C and polycrystalline at 350-900°C.

If the substrate has a single crystal and there is epitaxial growth when the coating exceeds 900°C, it will become a single crystal but since no hydrogen or halogen elements were added, it is not /127 possible to obtain a single crystal semiconductor with the configuration in this invention. This invention involves a product that has a completely different classification.

The primary feature of this invention is the production of an amorphous coating. For this amorphous coating, N-type conductive impurities with concentrations of 10^{14}-$10^{22}cm^{-3}$ in a phosphorus or

arsenic semiconductor were mixed with phosphine (PH_3) or arsine (AsH_3) to form the N-type semiconductor. On the other hand, if the same level of concentration diborane (B_2H_6) was added, a P-type semiconductor was produced. If these impurities were not added at all, it became an intrinsic semiconductor or a basically intrinsic semiconductor due to the addition of only background level impurities. Materials other than silicon forming a semiconductor on this amorphous coating include hydrogen, heavy hydrogen or halogen elements such as chlorine in concentrations of 0.2-200atomic%.

This eliminates silicon bond failure as well as the generation of a recombination center while causing an electrical neutralizing action. Addition of hydrogen or halogen to the semiconductor coating and simultaneous or subsequent coating formation is an essential part of this invention. With this invention, the addition of impurities to neutralize the recombination center is used in the process to complete the activation of hydrogen or halogen simultaneously added for activation of the electrically reactive gases.

For embodiment examples of this invention, carbon, nitrogen and oxygen were added for uniform dispersal in the semiconductor. CH_4, H_2H_6 were used as the carbon. Ammonia (NH_3) and hydrazine (N_2H_4) were the nitrogens and H_2O or O_2 were the oxygens. H_2O, NO_2, CH_3OH and other alcohols, CO_2 and CO were added to the reactor using hydrogen as the carrier gas. Two or more of the nitrogens and oxygens, or carbons and oxygens can be added. After formation of a single crystal semiconductor coating with oxygen or nitrogen, it becomes silicon oxide (Eg=8eV) or silicon nitride (Eg=5.5eV), not an insulation. Since these additives are actually added via electricity or electricity and

heat at the same time as production of the silicon coating, according to the stoichiometric ratio of these additives, the semiconductor produces values in the range of 1.1eV to 3eV (SiC), 5.5eV (Si_3N_4), 8eV (SiO). The Eg of this coating was measured by a monochromator or by the photoexcitation method.

Since this Eg has an amorphous structure for the two semiconductors, there is no Ns property at the heterojunction and the energy band that is a conductive band and a valence band that is abrupt and independent becomes smooth and continuous.

The Eg level at the varying junctions can be adjusted to a coating formation speed of 0.1-10μ/minute. The amount of doping additive can be turned ON/OFF or is produced for adjustment in continuous steps. An important aspect is that the boundary or area around these varying Eg is attributed to the production process but there is no Ns created due to the incommensurate lattice seen in the heterojunction of a single crystal semiconductor. Additionally, the conductive band and valence band of the Eg edge does not have notches or spikes. They are essentially nonexistent. It is believed that this is due to the stoichiometric ratio of these hydrogen or halogen impurities used as additives.

With this invention, one of the two semiconductors with varying Eg is a pure semiconductor while the other is a semiconductor with additives but this is not necessary. The amount of any of the same additives can be changed. For example, this invention is possible if one is 10^{15}-$10^{18}cm^{-3}$ and the other is 0.01-30atomic%. It is also acceptable if the carbide that is 10^{15}-$10^{22}cm^{-3}$ is changed to an additive with 5-10atomic%.

As clearly shown by the above theory, processes and results, this invention involves the critical junctions and their surrounding areas of semiconductor operation. Depending on the junction of the varying Eg materials, the interface notches and spikes found in existing devices have been eliminated. In other words, the lattice constant materials have essentially been eliminated. Thus, the important /128 aspect of this invention is an amorphous semiconductor where the incommensurate lattice is eliminated.

With this amorphous structure, the recombination center is neutralized by the hydrogen or halogen. Thus according to the stoichiometric ratio, the energy gap is continuously altered, which succeeds in providing a semiconductor device with a continuous junction.

Figure 2 is an embodiment example where the Eg is altered.

Figure 2(A) is of the junction where the amorphous semiconductor (11) is an N-type with a wide Eg (a wide energy gap is hereafter abbreviated as W). The amorphous semiconductor (13) is a P-type with a narrow Eg (a narrow energy gap is hereafter abbreviated as N, but differentiated from an N-type). Figure 2(B) is the same P-type semiconductor where the amorphous semiconductor (11) has W-Eg while the amorphous semiconductor (14) has N-Eg. Figure 2(C) is an NP junction. Figure 2(E) shows the NP junction structure with a smooth connection. Figure 2(F) shows a step NP junction structure.

Figure 3 shows one semiconductor with 2 junctions. Figure 3(A) is a W-L-W NPN transistor. In L of the P-type, the load Eg stimulates recombination. Figure 3(B) is a L-W-L PNP transistor. Figure 3(C) has a L-W-L NIP structure while Fig. 3(D) has a W-W-L PIN structure. With

this W value, a high level of conversion efficiency (1.5-3.0%) can be expected relative to the photocell light exposure. Figure 3(E) is a W-W-L NPN and Fig. 3(F) is a L-W-W PNP transistor.

With this invention, two semiconductors of different conductive types are constructed with varying energy bands. With identical conductive types or with either a P-type or an N-type impurity concentration, the Eg varies but this invention presents a semiconductor where the Eg varies continuously or in steps.

The additive can be determined according to the objective as shown in Fig. 2 and Fig. 3. These are merely a means to industrially promote this invention.

This invention is supplemented by providing specific examples.

Example 1

Using a plasma vapor reaction process, a junction with the structure shown in Figure 2(D) was produced. After the reaction reached a vacuum level of 0.001torr, a stainless steel substrate was maintained on a susceptor. This was subject to reactive gas at 13.56MHZ of high frequency heating and a reaction pressure of 0.3torr. The reactive gas was SiH_4. An amorphous semiconductor with added hydrogen was formed in a thickness of 0.5μ. Next, 20% of CH_4 relative to silane was added such that $CH_4/SiH_4=1$, $B_2H_6/SiH_4=1\%$. The second amorphous semiconductor was produced in a thickness of 0.5μ.

The optical energy band width for each amorphous semiconductor was measured using a monochromator as 1.6eV and 2.2eV. As indicated above, this is a two layered semiconductor where voltage is applied between the substrate and the electrode formed by vapor deposition of aluminum on the second semiconductor. There is a PI junction so it was

observed that the diode properties varied from 0-±5V. From these diode properties, the energy band exhibited a current leakage of less than 1.8mA in the forward direction and less than 10mA in the reverse direction with ±1V applied in an electrode area of 1mmΦ. When the P-type second semiconductor layer was formed, if the methane and silane were not added simultaneously, this value was 103 times less than the reverse direction leak when compared to the PI junction. When considering the forward direction current of 1/7 0.26mA, the junction properties improved and the energy band in the transition area was deemed to have a continuous effect.

As clearly indicated in the description above, this invention is for a semiconductor, where the embodiment example primarily utilized silicon. However, this invention is not limited solely to silicon, and germanium or silicon carbide can be utilized for the /129 semiconductor device. For practical purposes, the base materials used to neutralize the Ns in the amorphous semiconductor were halogen elements such as hydrogen or chloride with 0.1-200atomic%. The oxygen, nitrogen or carbon additives had a stoichiometric range of 10^{15}-$10^{18}cm^{-3}$. With carbon at 0.1-80%, nitrogen at 0.01-10% and oxygen at 10^{15}-$10^{18}cm^{-3}$, various adjustments were made either continuously or step-wise. As a result, semiconductors with varying Eg were adjacent but Ns generation due to incommensurate lattice was avoided. The P-type, N-type and I-type and their degree of conduction varied according to the type and amount of impurity added. This type of semiconductor device can be mass produced and can be produced using glow discharge for continuous production or chemical vapor deposition (CVD). The thickness of a single semiconductor can be controlled in a range of

0.01-10μ. The concentration of impurities in the P-type or N-type can be controlled in a range of 10^{14}-$10^{22}cm^{-3}$. The PN junction, PI junction, NI junction and PNP,PIN multi-layered junctions can be easily produced. Mass production can be continuously conducted in the same reactor so this has great implications for a completely new industrial field.

4. Brief Description of the Diagrams

Figure 1 shows energy bands for existing heterojunctions.

Figure 2 and Figure 3 show the embodiment examples for this invention.

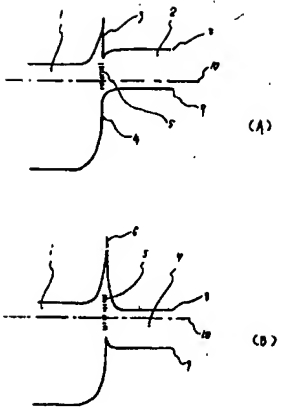

Figure 1

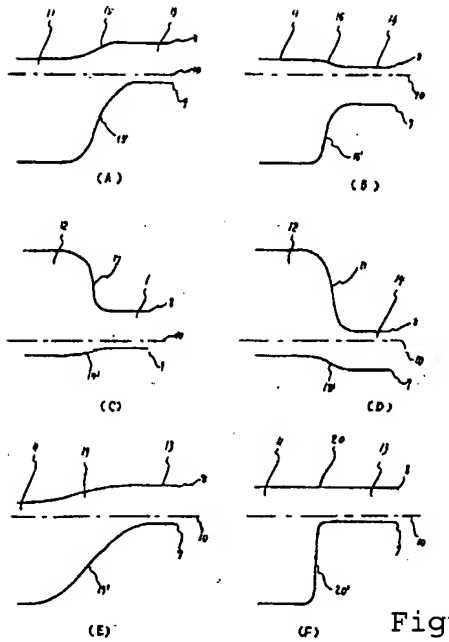

Figure 2

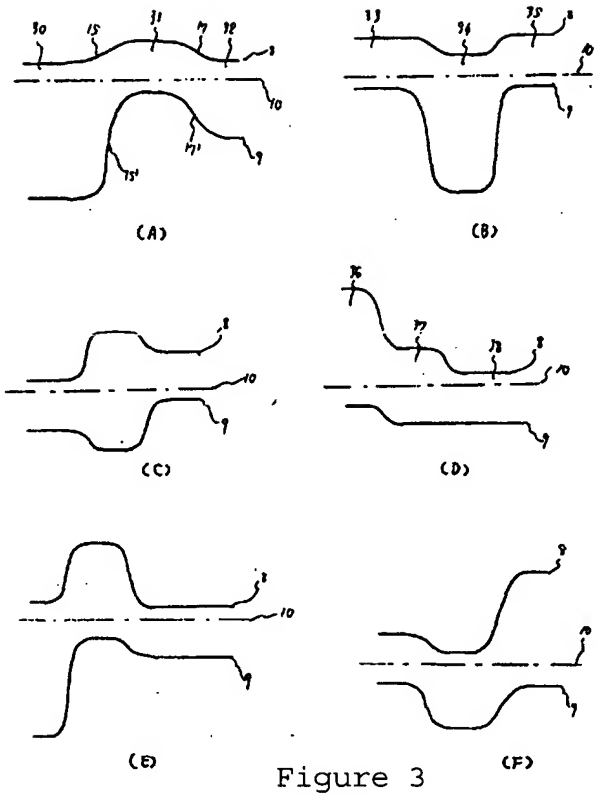

Figure 3